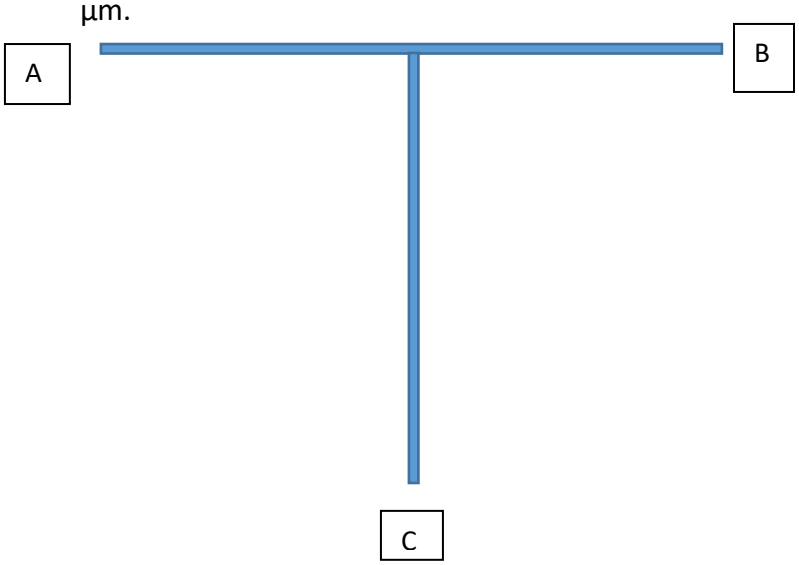
EE222 Midterm Examination

February 6, 2018

Name_____ Student ID_____

1. (20 points) For low power operation of CMOS circuits, **describe the design principle** in terms of power supply voltage V_{DD}, voltage swing ΔV at output nodes, switched capacitance C_{sw}(= product of switching frequency and capacitance), and MOST's threshold voltage V_T.

2. (20 points) Let us consider a T shape metal interconnect configuration of a uniform width 1 µm that connects three gates. Its horizontal length from point A to point B is 1000 µm and its vertical length starting at the center of the horizontal line is also 1000 µm long ending at point C.
   Assuming that the line resistance is 0.1 Ω/square, and line capacitance including the fringing field effect is 0.066 fF/ μm^2, **find an Elmore delay from the top left corner point A to the bottom most point C.** Use a distributed L-type RC model for every 250 µm.



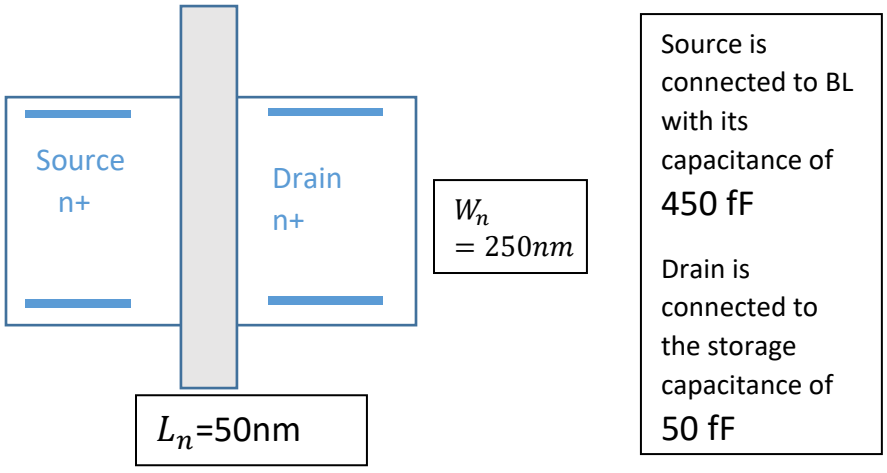
3. (30 points) A super buffer can be used to drive a large load capacitance C_{load} instead of abruptly enlarging the driving gate's transistor sizes. When the gate capacitance of an intrinsic inverter is C_g =0.166 fF and C_{load}= 3.655 pF,
   find a minimum delay in picoseconds. Here the intrinsic inverter's delay $\tau_o$is calculated from a 11-stage ring oscillator that has a frequency of 90.9 GHz.
   (Hint: Find τ_o from the oscillation frequency as f= 1/(2 X $11\tau_o$). Also C_{load}/C_g = e^{10} with e= 2.718.)

4. **after wordline (gate voltage) is switched to $2V_{DD}$.** (30 points) A dynamic random access memory (DRAM) cell is connected to its bitline (BL) with a total capacitance of 450 fF. The physical dimensions of the DRAM cell's NMOS transistor is shown below. The current driving power $\boldsymbol{I_{DS}}$ is described below. Let us assume that $V_{DD} = 2V$ and V_{Tn}= 0.5 V, $C_{storage}$= 50 fF. **Find the time it takes for BL, which was precharged to $\frac{V_{DD}}{2}$ by a precharge pulse while $C_{storage}$ was charged to V_{DD}, to reach the beginning of a steady state value after the wordline (WL) signal which is the gate voltage of NMOS transistor is switched to $2V_{DD}$.**

For simple calculation, assume that the parasitic drain capacitance can be neglected, and WL is driven with a high voltage 2 V_{DD} such that the NMOST is in its linear region, i.e.,

$$\boldsymbol{I_{DS} = k_n' W_n/L_n \frac{1}{1+\frac{V_{DS}}{E_C L_n}} ((V_{GS} - V_{Tn}) V_{DS} - ½ V_{DS}^2),}$$

where E_C= 10^5V/cm, L_n = 0.05 µm. The average value of $I_{DS} = \frac{1}{2}(I_{DS}$ for V_{DS}= 2V + I_{DS} for V_{DS}= steady state value) can be used for calculation of the delay.



(for problem 4 continuation)